or more clock signals, each capable of oscillating at a different one of a plurality of frequencies. The clock signals may be generated in response to (i) a reference clock (ii) the one or more control signals, and (iii) one or more of the clock signals. The programmable logic circuit and the phase lock loop circuit may be integrated on a single circuit.

CLAIM REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

The rejection of claims 3 and 4 under 35 U.S.C. §112, first paragraph is respectfully traversed in part and has been obviated, in part, by appropriate amendment. As such, the rejection should be withdrawn.

Applicants' representative disagrees with the Examiner's statement that no evidence of knowledge in the art of programmable logic devices has been provided (page 2, lines 23+, of the office action). FIG. 3 of the present application discloses an example of a programmable logic circuit. The programmable logic circuit of FIG. 3 comprises a number of logic blocks. A person of ordinary skill in the art of programmable logic devices would know that the logic blocks of FIG. 3 could contain a product term array. The programmable logic device section of the Cypress Data Book 1996 evidences that one of ordinary skill in the art would know that the logic blocks of FIG. 3 can comprise a product term array. The programmable logic device section of the Cypress Data Book 1996 was

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submitted in an Information Disclosure Statement filed with the present application. The acknowledgment of this submission can be found in the initialed PTO-1449 form attached to Paper No. 4. Claim 4 is amended to appease the Examiner and advance prosecution (see page 2, lines 21-23 of the office action).

Furthermore, one skilled in the art would be able to make and/or use the presently claimed invention without undue experimentation, in light of the specification as originally filed. Therefore, the presently pending invention is fully described and enabled within the meaning of 35 U.S.C. § 112, first paragraph. As such, the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 2, 6, 10, 12, 15-16, 18, and 20-23 under 35 U.S.C. § 102(e) as being anticipated by Chou et al. is respectfully traversed and should be withdrawn. The rejection of claims 22-23 under 35 U.S.C. § 102(e) as being anticipated by Weiss et al. has been obviated by appropriate amendment and should be withdrawn.

According to the Office Action, Chou et al. teach a programmable logic circuit (elements 6, 8, and 9 of FIG. 5 of Chou et al.) and a phase lock loop (elements 2, 3, and 4 of FIG. 5 of Chou et al.). The phase lock loop, as defined by the Office Action, generates an output in response to two inputs received from

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the programmable logic circuit. The phase lock loop circuit (elements 2, 3, and 4 of FIG. 5 of Chou) does not appear to generate one or more clock signals in response to (i) a reference clock, (ii) one or more control signals from the programmable logic circuit, and (iii) one or more of the clock signals, as is presently claimed.

In contrast, the presently claimed invention provides a programmable logic circuit and a phase lock loop circuit. The programmable logic circuit may be configured to (i) generate one or more control signals and (ii) receive one or more clock signals. The phase lock loop circuit may be configured to generate the one or more clock signals, each capable of oscillating at a different one of a plurality of frequencies. The clock signals may be generated in response to (i) a reference clock (ii) the one or more control signals, and (iii) one or more of the clock signals.

Chou et al., as interpreted by the Examiner, fail to disclose a phase lock loop circuit configured to generate one or more clock signals in response to (i) a reference clock, (ii) one or more control signals, and (iii) one or more of the clock signals, as is presently claimed. In addition, if the phase lock loop circuit of Chou et al. is interpreted as including the counter 6 and the counter 9, an interpretation that is supported by the Examiner's own art (see FIG. 1 and col. 1, lines 15-27 of Chou et al.; FIG. 4 and col. 10, lines 4-6 of Davis et al.), Chou et al.

fail to disclose a programmable logic circuit configured to receive one or more clock signals, as is presently claimed. Therefore, Chou et al. fail to disclose or suggest all the elements of the presently claimed invention. As such, the presently pending claims are believed to be fully patentable over the cited reference and the rejection should be withdrawn.

With respect to claims 22-23, Weiss et al. disclose a data processing system having a register controllable speed (Title). FIG. 4 of Weiss et al. shows a clock input **divided** into a number of clocks by the dividers block 404. Binary data stored in registers is used by a 4-to-16 line decoder to **select** one of the number of clocks (FIGS. 4 and 5, and column 1, lines 43-49, of Weiss et al.). Weiss et al. appear silent with regard to generating one or more clock signals in response to (i) a reference clock, (ii) **one or more of the clock signals**, and one or more control signals.

Weiss et al. do not disclose or suggest a means for generating the one or more clock signals in response to a reference clock, one or more of the clock signals and one or more control signals, as presently claimed. Therefore, Weiss et al. do not disclose or suggest all the elements of the presently claimed invention. As such, the presently claimed invention is believed to be fully patentable over the cited reference and the rejection should be withdrawn.

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CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 7-9, and 19 as being unpatentable over Chou et al. in view of Davis et al. and claims 5, 17, and 24 as being unpatentable over Chou et al. in view of Appel is respectfully traversed and should be withdrawn. Claims 5, 7-9, 17, 19, and 24 depend, either directly or indirectly, from the independent claims 12 and 15, which are believed to be allowable. As such, the presently pending claims 5, 7-9, 17, 19 and 24 are also believed to be fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

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If any additional fees are due, please charge our office Account No. 02-2712.

Respectfully submitted,

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